TIMING AND VOLTAGE CONTROL OF MAGNETIC MODULATORS ON ETA II*

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Abstract

The Experimental Test Accelerator II is a high-average-power, high-repetition-rate linear induction accelerator at Lawrence Livermore National Laboratory. Magnetic pulse compressors are used in the power conditioning chains that produce pulses used to accelerate the electron beam. Stable operation of each power-conditioning chain is essential to overall accelerator performance. Variations in voltage or timing ("jitter") of pulses driving the induction cells can cause unacceptable variations in electron-beam energy. This paper reviews techniques developed and implemented to regulate voltage and to control sources of timing jitter. These techniques have demonstrated subnanosecond jitter and ±0.1% pulse-to-pulse voltage regulation of the accelerator drive pulses.

Introduction

The Experimental Test Accelerator II (ETA II), a high-average-power linear-induction accelerator at Lawrence Livermore National Laboratory, generates a 6-MeV, 3-kA electron beam at a 5-kHz pulse repetition rate. Four power conditioning chains based on magnetic pulse compressors generate the 110-kV, 70-ns pulses used to accelerate the electron beam. For each chain, precise timing and voltage control of the accelerator drive pulses are essential for stable and repeatable accelerator operation. Excessive variations in pulse voltage or timing ("jitter") cause unacceptable variations in electron-beam energy. In this paper we discuss two methods for controlling jitter: voltage regulation and delay compensation. We also analyze the limitations of these methods and present operational results.

Figure 1 is a block diagram of the ETA II power conditioning system. Each of four power conditioning chains consists of a dc power supply and capacitor bank, thyratron modulator, and a magnetic pulse compressor dubbed the MAG-1-D. The modulator charges the input of the MAG-1-D, which, in turn, drives a set of 20 induction cells or the injector.

The thyratron modulators, shown in Fig. 2, use a command resonant charge and de-Qing circuit to charge and regulate the voltage on the intermediate energy storage capacitor, C_2. Thyratrons discharge the energy stored in C_2 into the input of the MAG-1-D. The amplitude and timing of the output of each thyratron modulator must be strictly regulated for the electron beam to exhibit the desired pulse-to-pulse and intrapulse energy regulation. The voltage in each modulator is regulated independently of the others to maintain the pulse-to-pulse beam energy regulation. In addition, a delay compensation circuit is used to reduce timing jitter by decreasing voltage-dependent timing variations in the magnetic modulator.
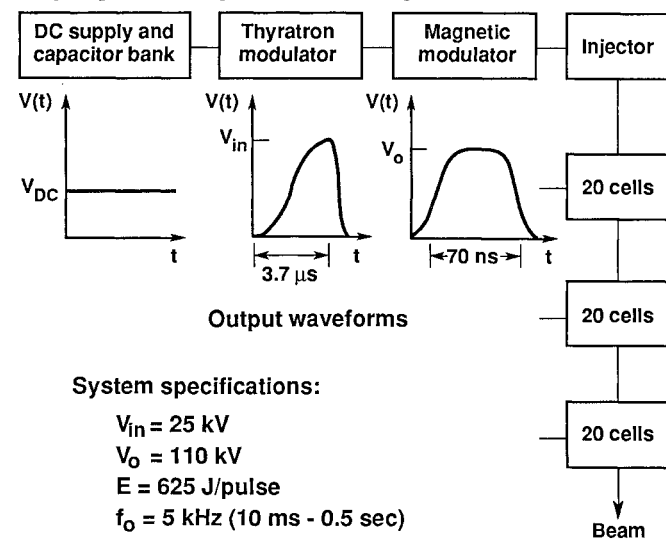

Output waveforms

System specifications:

V_{in} = 25 kV

V_O = 110 kV

E = 625 J/pulse

f_O = 5 kHz (10 ms - 0.5 sec)

Figure 1. Block diagram of the ETA II power conditioning system.

Voltage Regulation

The MAG-1-D input voltage must be regulated to within ±0.1% for ETA II to exhibit acceptable pulse-to-pulse variations in beam energy. Voltages on each chain are regulated by de-Qing the charging inductor, L, in the command resonant charge circuit, as shown in Fig. 2. The de-Qing process is as follows: The voltage on C_2 is regulated by comparing it to a reference voltage and triggering S_2 when C_2 has reached the desired voltage. When S_2 is triggered (at t_{dq}) the voltage across L is instantaneously reduced and S_1 is reverse biased for the interval $\pi/2 < \omega t_{dq} < \pi$. Since S_1 will only conduct current in one direction, the charging current stops flowing and C_2 remains at the desired voltage.
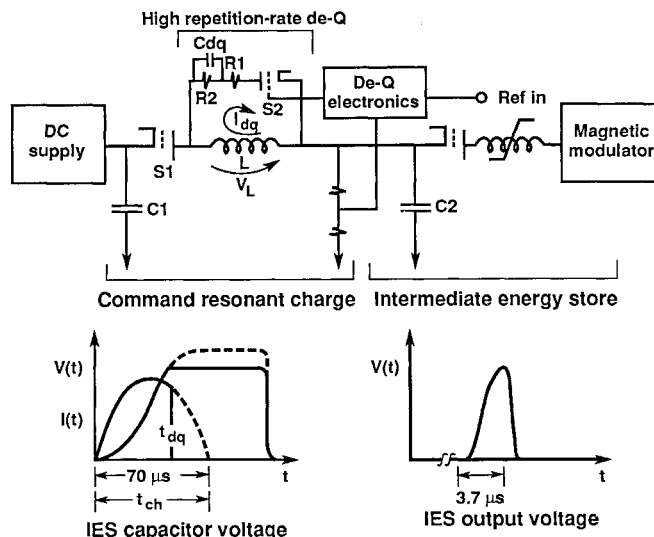

Figure 2. Thyratron modulator incorporating the de-Qing circuit.

One of the more difficult aspects of achieving ±0.1% regulation is compensating for droop in the power supply/capacitor bank voltage during the first 30 ms of operation. For a 1000-μF capacitor bank (per chain), the predicted power supply voltage droop during the first 30 ms is approximately 14%. There is a fixed delay of approximately 1 μs from the time that the correct voltage level is detected on C_2 until the time that the de-Qing switch, S_2, begins to conduct current. The voltage change on C_2 during this delay time decreases from pulse to pulse. To compensate for changes resulting from the capacitor-bank loop, we correct the measured signal with a signal that is proportional to the slope of the C_2 voltage waveform. The voltage on C_2 is measured differentially with two high-impedance voltage probes. The differential voltage signal is then corrected by summing it with the derivative of the C_2 voltage, which phase shifts the measured voltage waveform earlier in time. The amount of phase shift required is determined by the amount of delay in the de-Qing circuit, $\emptyset = \omega t_{delay}$, where ω is the charge frequency and t_{delay} is the inherent delay in triggering the de-Qing switch. When the phase shift is set correctly, the voltage on C_2 when the de-Qing switch begins to conduct will equal the desired voltage.

Figure 3 shows ±0.04% voltage regulation on ETA II with resistive de-Qing at 1 Hz. The power supply droop was simulated in the picture by changing the power supply voltage by 7%. For high-repetition-rate operation, however, a simple resistive network could not simultaneously satisify both the repetition-rate requirement ($5L/R_{dq} < 1/f_o - t_{ch}$) and the voltage regulation requirement ($R_{dq} < V_L/I_L$) for 20% input-voltage variations. The high-repetition-rate requirement would set $R_{dq} > 9.5\ \Omega$, whereas the voltage-regulation requirement would set $R_{dq} < 5\ \Omega$. Therefore,

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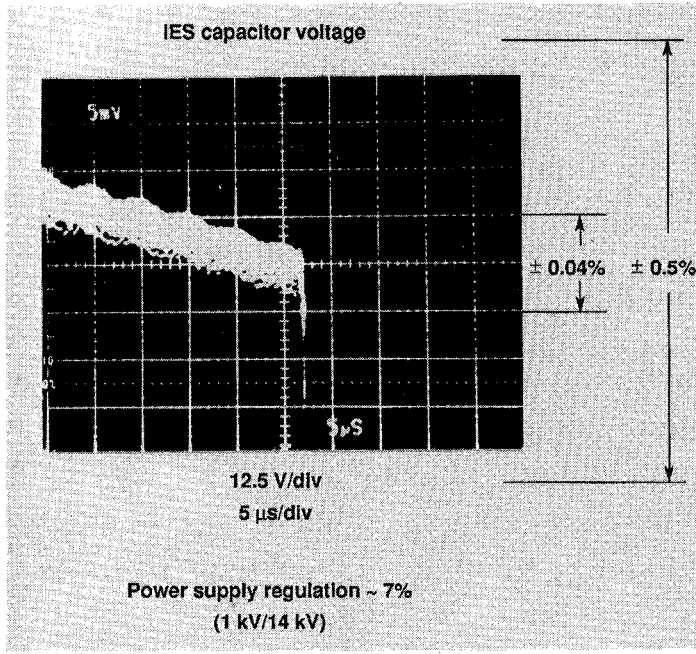| 15. SUBJECT TERMS					
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Figure 3. IES capacitor voltage at time of fire.

we use a resistive-capacitive network for high-repetition-rate de-Qing (Fig. 2). For ETA II requirements, the network shown in Fig. 2 would satisfy both requirements with $R_1 = 2 \Omega$, $R_2 = 6 \Omega$ and $C_{dq} = 4 \mu f$.

We have done computer simulations of de-Qing network behavior on ETA II. Figure 4 shows waveforms produced by these simulations. The simulations show that current flowing in the de-Qing network decays to zero in less than 200 μs, thus satisfying the 5-kHz operating requirement. Also, the circuit regulates near $\omega t = \pi/2$, thus regulating the input voltage over the required 20% range. The currents and voltages in the de-Qing network are given by

$$i_{dq}(t) = I_L(t_{dq}) \left[e^{-\alpha t} \cos \beta t + \frac{(b_1 - a_1 \alpha)}{\beta} e^{-\alpha t} \sin \beta t \right] ,$$

$$V_L(t) = I_L(t_{dq}) \left\{ R_1 e^{-\alpha t} \cos \beta t + \frac{1}{\beta}[(R_1 + R_2)b_1 - R_1\alpha]e^{-\alpha t} \sin \beta t \right\} ,$$

where

$I_L(t_{dq})$ = current flowing in L at t_{dq},

$$\alpha = \frac{L + R_1 R_2 C_{dq}}{2LR_2 C_{dq}},$$

$$\beta^2 = \frac{R_1 + R_2}{R_2 LC_{dq}} - \left(\frac{L + R_1 R_2 C_{dq}}{2LR_2 C_{dq}}\right)^2 ,$$

$$a_1 = 1$$
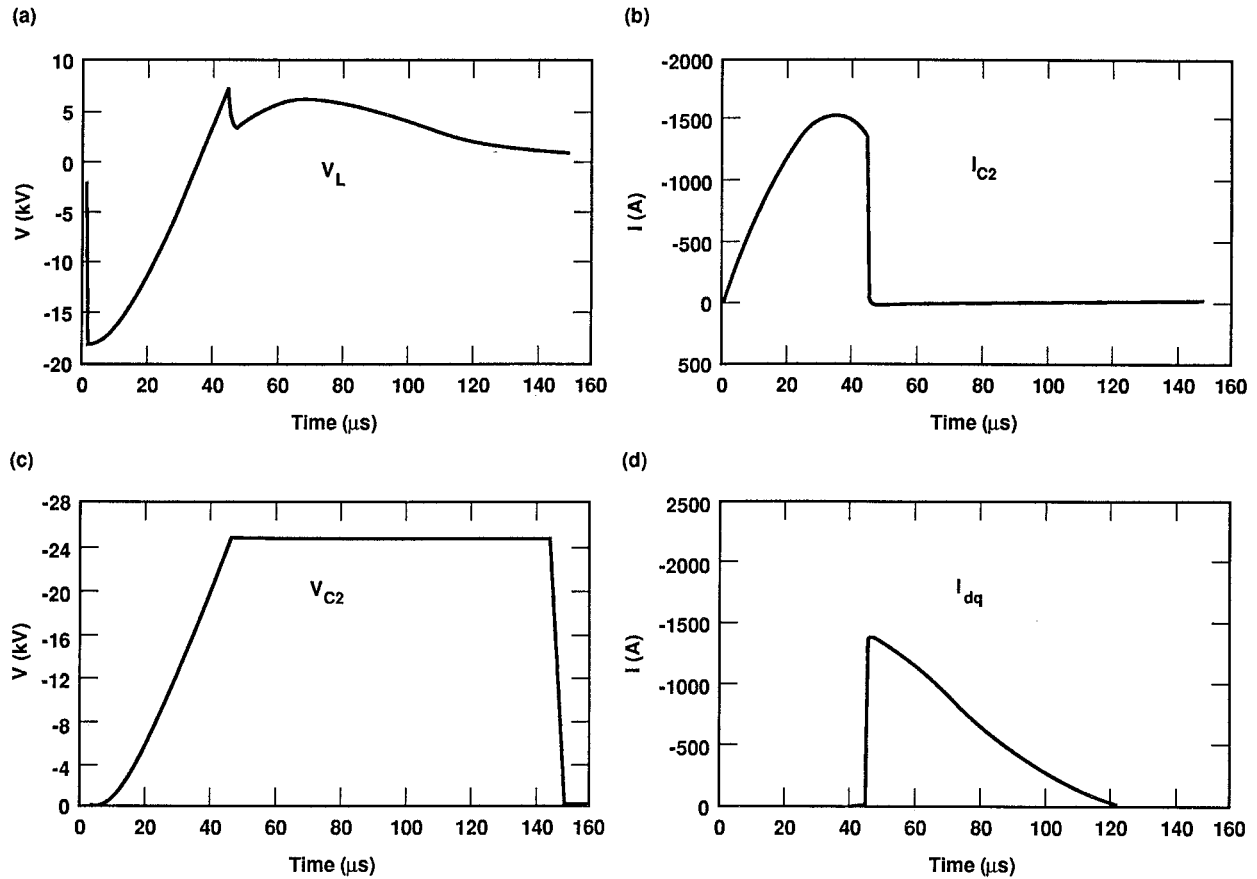
$$b_1 = \frac{1}{R_2 C}$$

Figure 4. De-Qing waveforms for the resistive-capacitive network. (a) Inductor voltage. (b) Charge current. (c) Intermediate energy store capacitor voltage. (d) De-Qing current.

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Since the de-Qing network dissipates all energy stored in the charging inductor at the time of de-Qing, the power dissipation in the de-Qing resistors can be expressed as

$$P_{\text{diss}} = f_0 E_{\text{IES}} \left(\frac{2V_{\text{CO}}}{V_{\text{CIES}}} - 1 \right) ,$$

where

f_0 = repetition rate,
E_{IES} = energy stored in C_2,
V_{CO} = voltage on power supply/capacitor bank,
V_{CIES} = desired voltage on IES capacitor.

Delay Compensation

Voltage variations of ± 0.1% on the input to the MAG-1-D would result in output pulse timing variations of ± 2.5 ns. However, each power-conditioning chain must exhibit subnanosecond timing variations, which, in turn, would require better-than ±0.02% voltage regulation on the input to the MAG-1-D. To relax the voltage regulation requirement, a delay compensation circuit (Fig. 5) was developed to decrease the sensitivity of the modulator system timing to voltage variations. This circuit changes the trigger delay in the modulator system as a function of the input voltage. Figure 5 shows the time delay vs input voltage characteristic of both the delay circuit and the MAG-1-D. For small voltage changes, the net timing variation through the modulator system arising from variations in input voltage is reduced because the characteristic curves of the compensation circuit and MAG-1-D have equal and opposite slopes at the operating point.

The delay compensation circuit uses a linear ramp to approximate the nonlinear volt-time characteristic curve of the magnetic modulator. This approximation limits the maximum input voltage regulation that can be compensated while maintaining subnanosecond system jitter. The achievable jitter reduction can be approximated as

$$e_t = \frac{e_v^2}{2} (1 - e_v) ,$$

where e_t is the percent timing variation resulting from e_v, the percent input voltage variation. In addition, an improvement factor $I = 1/e_v$ can be used to estimate the reduction in timing variation that can be expected with a given value of voltage regulation.

Figure 6 compares system delay vs input charge voltage on an ETA II modulator system both with and without delay compensation. With compensation, delay time is much less sensitive to voltage variations. Figure 7 shows the reduction in timing variations achieved using delay compensation. We have implemented this technique on the four modulator systems on ETA II and have achieved total system jitters of 600 ps (1σ).
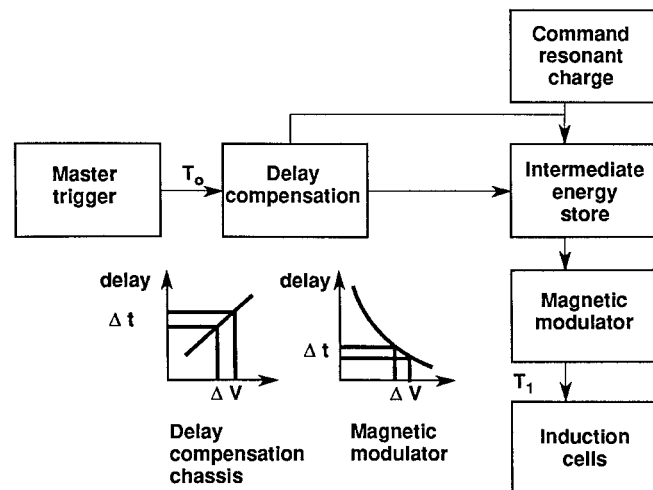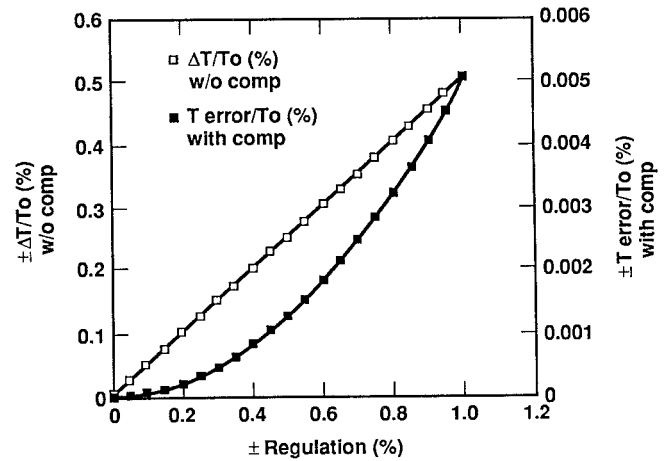

Figure 6. Comparison of compensated and uncompensated modulator system delays.
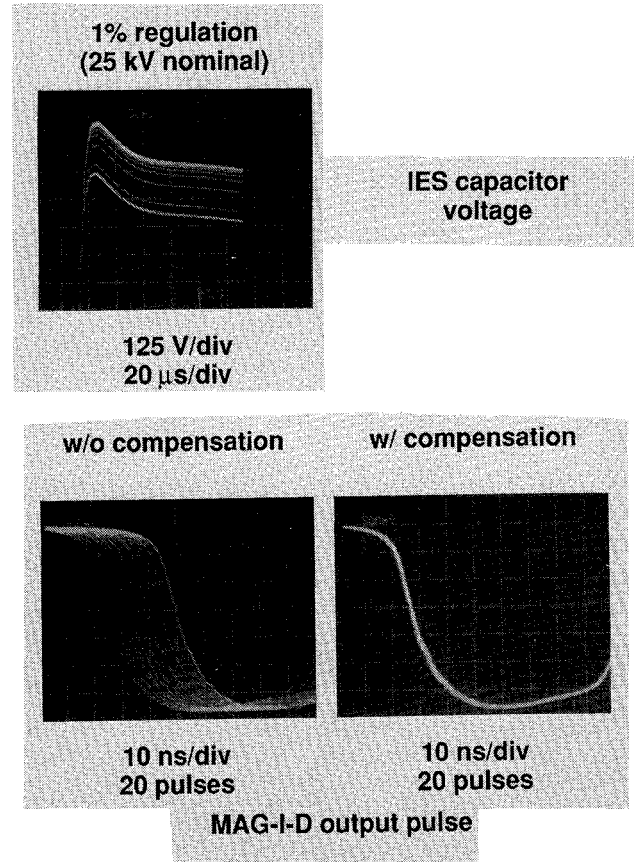

Figure 7. Reduction of output pulse jitter with delay compensation.

Summary

We have used both voltage regulation and delay compensation techniques to control jitter on ETA II. To maintain system jitters of less than 1 ns (1σ), the voltage input to the MAG-1-D pulse compressor must be tightly regulated. To ease this requirement, we implemented a delay compensation technique that reduced timing variations by at least a factor of 10 for voltage variations of 1%. In addition, voltage regulations of ±0.04% have been achieved on ETA II at 1 Hz. The high-repetition-rate de-Qing design is currently being implemented on ETA II.

Figure 5. Block diagram of delay compensation circuit.

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